Enrollment No: _____ Exam Seat No:_____

C.U.SHAH UNIVERSITY

Summer Examination-2017

Subject Name: Advance Embedded System

Subject Code: 5TE02AES1 **Branch: M.Tech(VESD)**

Semester: 2 **Date: 06/05/2017** **Time: 02:00 To 05:00** **Marks: 70**

Instructions:

(1) Use of Programmable calculator & any other electronic instrument is prohibited.
(2) Instructions written on main answer book are strictly to be obeyed.
(3) Draw neat diagrams and figures (if necessary) at right places.
(4) Assume suitable data if needed.

SECTION – I

Q-1		**Attempt the Following questions**	**(07)**
	a.	Define the term "general purpose processor"?	**1**
	b.	Define the term "Single purpose processor"?	**1**
	c.	Draw the basic architecture of general purpose processor.	**1**
	d.	What is the main difference between a synchronous and an asynchronous circuit?	**1**
	e.	What is purpose of datapath in general purpose processor?	**1**
	f.	What is purpose of datapath in single purpose processor?	**1**
	g.	Why embedded system designer choose custom single purpose processor rather than a general purpose processor?	**1**
Q-2		**Attempt all questions**	**(14)**
	a)	Explain Combinational logic design process with example.	**5**
	b)	Explain in detail RT – level custom single purpose processor design.	**5**
	c)	Explain in brief with diagram standard software development process.	**4**
		OR	
Q-2		**Attempt all questions**	**(14)**
	a)	Explain Sequential logic design process with example.	**5**
	b)	Enlist different optimizing techniques. Explain any two of them in detail.	**5**
	c)	Explain in brief ASIPs.	**4**
Q-3		**Attempt all questions**	**(14)**
	a)	State different types of RAM and explain each of them in detail.	**7**
	b)	Explain in detail composing memory with example. Draw the memory hierarchy.	**7**
		OR	
Q-3	**a)**	State different types of ROM and explain each of them in detail.	**7**
	b)	Enlist different advanced RAM. Explain each of them in detail.	**7**

SECTION – II

Q-4		**Attempt the Following questions**	**(07)**
	a.	Why cost of the general purpose processor is less than that of single purpose processor	**1**

		you design yourself?	
	b.	Explain in brief cache memory.	**1**
	c.	Explain in brief with diagram Princeton architecture	**1**
	d.	Explain in brief with diagram Harvard architecture	**1**
	e.	Explain in brief with diagram pipelining.	**1**
	f.	Explain in brief PSRAM.	**1**
	g.	Explain in brief NRAM.	**1**
Q-5		**Attempt all questions**	**(14)**
	a)	1. State and explain in brief different models used for describing an embedded system. 2. Explain in brief with example models v/s languages.	**7**
	b)	Explain HCFSM in detail with example.	**7**
		OR	**(14)**
Q-5	**a)**	Write a short note on capturing state machines in sequential programming language.	**7**
	b)	List and explain the mechanisms for synchronization among processes.	**7**
Q-6		**Attempt all questions**	**(14)**
	a)	Enlist the different levels of synthesis. Explain in detail each of them.	**7**
	b)	Explain CPU Accelerator in detail.	**7**
		OR	
Q-6		**Attempt all Questions**	**(14)**
	a)	1. What is Reuse? Explain IP cores and their forms in brief. 2. What are the challenges posed by IP cores to processor providers?	**7**
	b)	Explain in detail with diagram the system architecture of audio players.	**7**